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CLAIMS

What is claimed is:

1 1. An island photodiode comprising:

2 a core;

3 light sensing sidewalls along an exterior of said core; and

4 logic circuitry above said core.

1 2. The island photodiode in claim 1, wherein said sidewalls are perpendicular to a surface of
2 said photodiode that receives incident light.

1 3. The island photodiode in claim 1, wherein said light sensing sidewalls comprise a
2 junction region that causes electron transfer when struck with light.

1 4. The island photodiode in claim 1, wherein said logic circuitry blocks light from said core.

1 5. The island photodiode in claim 1, wherein said sidewalls comprise four vertical
2 sidewalls.

1 6. The island photodiode in claim 1, wherein said core comprises a n⁺ core and said
2 sidewalls comprise p⁺ sidewalls.

1 7. A photodiode array comprising:

2 a plurality of photodiode cores;

3 light sensing sidewalls along an exterior of said cores;

4 logic circuitry above said cores;

5 trenches separating said cores; and

6 a transparent material in said trenches.

1 8. The photodiode array pixel in claim 7, wherein said sidewalls are perpendicular to a
2 surface of said photodiode that receives incident light.

1 9. The photodiode array in claim 7, wherein said light sensing sidewalls comprise a junction
2 region that causes electron transfer when struck with light.

1 10. The photodiode array in claim 7, wherein said logic circuitry blocks light from said core.

1 11. The photodiode array in claim 7, wherein said sidewalls comprise four vertical sidewalls.

1 12. The photodiode array in claim 7, wherein said core comprises a n⁺ core and said
2 sidewalls comprise p⁺ sidewalls.

1 13. A p-i-n island photodiode comprising:
2 a n⁺ core having a cube shape;

1 an intrinsic layer surrounding sides of said n+ core;
2 a p+ layer surrounding sides of said intrinsic layer; and
3 at least one transistor above said n+ core.

1 14. The p-i-n island photodiode in claim 13, further comprising an n-well between and
2 connecting said n+ core and said transistor.

1 15. The p-i-n island photodiode in claim 13, wherein said p+ layer comprises a p-type doped
2 layer having a doping concentration in the range from $1e15$ to $1e18\text{ cm}^3$.

1 16. The p-i-n island photodiode in claim 13, wherein n+ core comprises an n-type doped
2 layer having a doping concentration in the range from $10e15$ to $10e17\text{ cm}^3$.

1 17. The p-i-n photo diode in claim 13, further comprising an anti-reflective coating
2 surrounding sides of said p+ layer.

1 18. The p-i-n photo diode in claim 13, further comprising a transparent material adjacent said
2 anti-reflective coating.

1 19. The p-i-n photo diode in claim 18, further comprising wiring levels above said transistor
2 and said transparent regions, wherein said wiring levels include transparent regions above said
3 transparent material.

1 20. A method of forming an island photodiode comprising:
2 forming a core in a substrate;
3 forming trenches in said substrate adjacent said core;
4 forming light sensing sidewalls along said trenches; and
5 forming logic circuitry above said core.

1 21. The method in claim 20, wherein said sidewalls are perpendicular to a surface of said
2 photodiode that receives incident light.

1 22. The method in claim 20, wherein said forming of said light sensing sidewalls comprises
2 doping sidewalls of said trench to form a junction region between said sidewalls and said core
3 that causes electron transfer when said sensing sidewalls are struck with light.

1 23. The method in claim 20, wherein said logic circuitry blocks light from said core.

1 24. The method in claim 20, wherein said forming of said trenches forms four vertical
2 sidewalls around said core.

1 25. The method in claim 20, further comprising doping said core with impurities to form an
2 n⁺ core and doping said sidewalls with impurities to form p⁺ sidewalls.

1 26. A method of forming an array of island photodiodes comprising:
2 forming cores in a substrate;
3 forming trenches in said substrate adjacent said cores;
4 forming light sensing sidewalls along said trenches; and
5 forming logic circuitry above each of said cores.

1 27. The method in claim 26, wherein said sidewalls are perpendicular to a surface of said
2 photodiode that receives incident light.

1 28. The method in claim 26, wherein said forming of said light sensing sidewalls comprises
2 doping sidewalls of said trench to form a junction region between said sidewalls and said cores
3 that causes electron transfer when said sensing sidewalls are struck with light.

1 29. The method in claim 26, wherein said logic circuitry blocks light from said cores.

1 30. The method in claim 26, wherein said forming of said trenches forms four vertical
2 sidewalls around each of said cores.

1 31. The method in claim 26, further comprising doping said cores with impurities to form an
2 n⁺ core and doping said sidewalls with impurities to form p⁺ sidewalls.